Advantages of NPC Inverter Topologies with Power Modules

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Efficiency is becoming increasingly important in power electronics. In many applications are running new projects driven by the initiatives for reduced energy consumption. The technology leaders are inverter applications in the solar market, but also uninterruptible power supplies and motor drives have new targets for improved efficiency. This paper shows alternatives for 3~ inverters with 700V DC-link voltage.

Operation modes of NPC

The sinusoidal output current and voltage is the same for NPC and half bridge. The difference is the way to generate the signal.

Example:
An inverter with 700V DC-voltage (+/-350V) generates and 3 phase output signal with $400V_{AC}$ phase to phase. The standard configuration with 3 halfbriges will switch the voltage from + 350V to -350V. For this operation are 1200V components needed. The disadvantages here are the following:

- The switching losses are the product of the total 700V and the output current.
- 1200V components are slower than 600V components
- output voltage ripple is high

The NPC inverter with 3 NPC-bridges will switch either +350V to 0V (positive half wave) or -300V to 0V (negative halve wave). Here are only 600V components needed. This generates the following advantages:

- The dynamic losses are significantly reduced, only 350V are switched.
- 600V components are faster and there are many ultrafast components available.
- The output ripple is reduced.
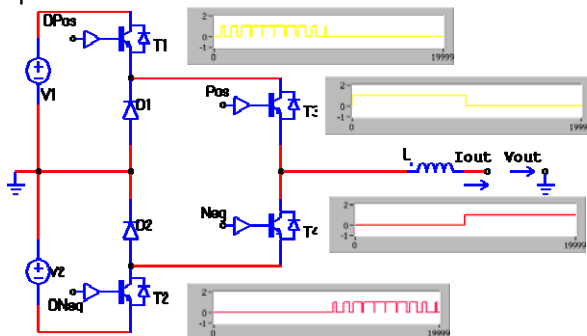
Operation Mode of NPC:

Fig. 1: The gate signal of a 3 level inverter at real power.

T3 is switched on during the positive halfwave of the output signal. T4 is switched on during the negative halfwave. The PWM is modulated with T1 and T2 (see Fig. 1). When T1 is switched off during the positive halfwave, the current will commutate from the neutral point through D1 to the output. The negative path is completely inactive. At the negative halfwave we have the same proceed with negative current but here is T1 and T3 inactive.

Advantages of NPC

The NPC topology offers the following advantages:

- Reduced switching losses:
  Only the half the voltage have to be switched this half's also the switching losses in the transistor. In the shown NPC topology we are able to use 600V components instead of 1200V types. On top on that are in 600V technology much faster components available than in 1200V technique. This will lead to further reduction of the switching losses.
- Smaller output current ripple:
  The NPC topology will have lower ripple in the output current and half of the output voltage transient. This will reduce the effort for filtering and isolation in the filter inductor.
- The total +/- supply voltage is shared:
  The DC voltage is divided in a positive and in a negative voltage which supports the serial connection of DC-capacitors without problems of leakage compensation.

These advantages have to face the drawback of a higher complexity. More components have to be handled (10 instead of 4) and the NPC topology requires 4 independent gate drives instead of 2 in the standard half bridge topology.

Challenges for NPC Power Modules

The NPC topology is distinguished with a higher complexity this makes the circuit more sensitive for parasitic effects. To avoid such disadvantages more care for the module design have to be taken.

In half bridge topologies is the low inductance between DC+ and DC- decisive. The same is valid for the NPC topology but here is additionally a low inductance between both DC voltages and the neutral point (NP) important. This task is hindered by the fact that more components are included.

The inductance of power module based circuits is mainly influenced by the wire bonds of the semiconductors and the external interconnection. The inductive loops inside the power module are largely canceled by the eddy current inducted into the backside metallization of the module. The current and commutation loops at real power are shown in Fig. 2.
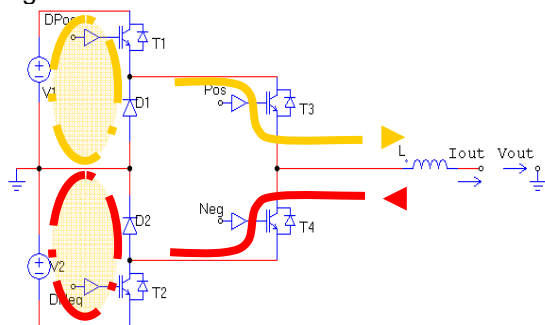

Fig. 2: Current and commutation loops at real power

The current and commutation loops at reactive power are shown in Fig. 3.
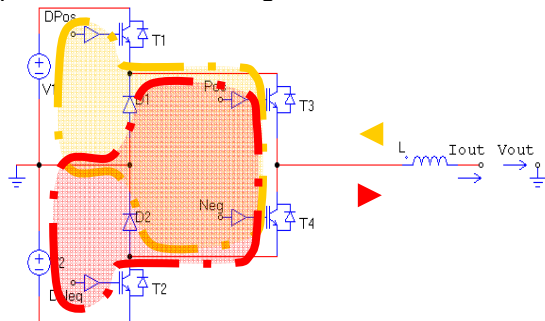

Fig. 3: Current and commutation loops at reactive power

The parasitics will increase the switch off losses of the transistors. Therefore the target is to minimize the inductance between DC+, DC- and NP. In Fig. 4 are the parasitic induction of a NPC power module shown.
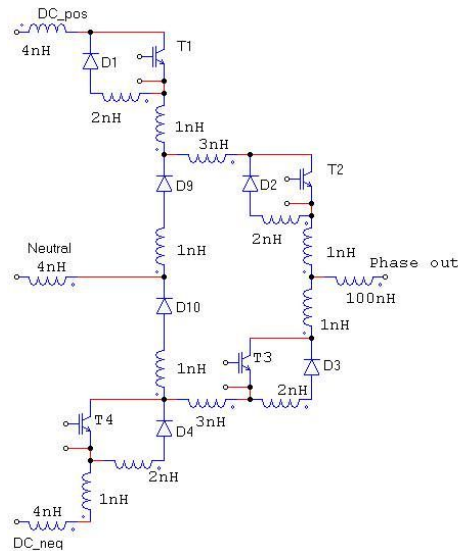

Fig. 4: Parasitic inductance of a 1200V-300A NPC module

The pinning of the module is the key for a reduction of the parasitic inductance outside of the module. In Fig. 5 is a pinning of a low inductive NPC module shown. The NP is here on both sides available to build on one side a low inductive pair with DC+ and on the other side with DC-.
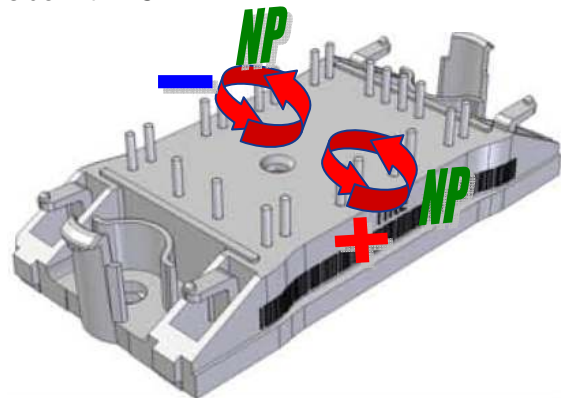

Fig. 5: Pinning of a low inductive 1200V-75A NPC module

Benchmark of the Topologies

In the following we made a benchmark of the topologies. In the comparison are standard half bridges (Fig. 6) are compared with the here discussed NPC topology (Fig. 7) and with a mixed voltage 3 level topology (Fig. 8).
The conditions of the comparison are following:

- 4,6kW Static load (25A) per phase
- 700V DC voltage (2*350V for 3 level)
- Output frequency 50Hz
- Modulation frequency = 16kHz
- Hard switching environment
- Sinusoidal output voltage waveform (230VAC)
- Sinusoidal output current waveform

- Cosfi=0,8
- 17,2kVA 3 phase power

The effort or chip area is given as the product of voltage rating and nominal current of the power semiconductor which is in line with the cost of the semiconductors.

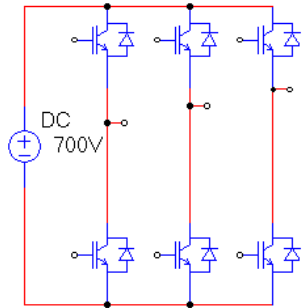The standard configuration for a 3 phase inverter are 3 half bridges.

Fig. 6: Standard inverter with 3 half bridges

The components are 2nd generation of 1200V trench field-stop IGBT´s with the corresponding freewheeling diodes. The result is following:

conduction losses:	36W
switching losses:	118W
total losses:	154W
efficiency:	96,65%
total rating of Si:	720kVA

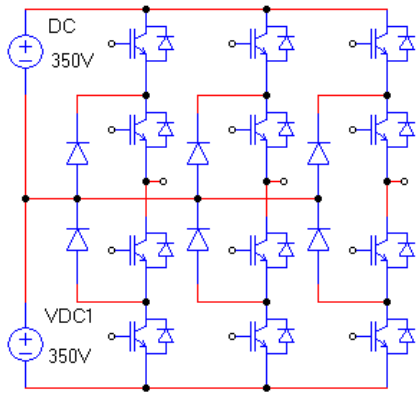The NPC topology is the next circuit to compare.

Fig. 7: NPC topology

The components are the first generation of 600V trench field-stop IGBT´s with the corresponding freewheeling diodes. Here the results:

conduction losses:	62W
switching losses:	28W
total losses:	90W
efficiency:	98,04%
total rating of Si:	900kVA

An additional 3 level topology is the mixed voltage 3 level topology. This circuit combines the low conductive losses of the half bridge solution with the advantages of switching only between DC+/- and the NP.
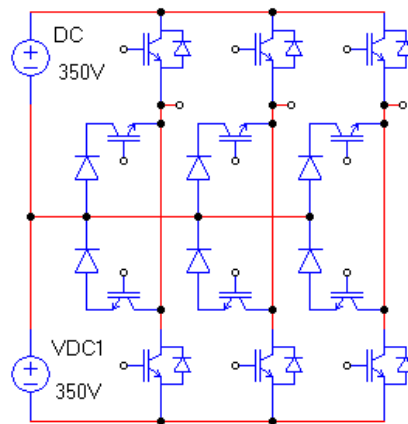

Fig. 8: Mixed voltage 3 level topology

The problem is here that the outside transistors have to be rated with 1200V, this reduces the switching performance to the level provided by 1200V components.
The components used in the benchmark are high speed 1200V IGBT´s and freewheeling diodes for the outside switches and the first generation of 600V trench field-stop IGBT´s with the corresponding freewheeling diodes for the NP-switches. However, here the results:

conduction losses:	50W
switching losses:	40W
total losses:	90W
efficiency:	98,04%
total rating of Si:	1080kVA

Result

The comparison shows that with both 3 level topologies are 98,04% efficiency achievable compared to 96,65% of the standard 3 phase bridge. The effort in semiconductor cost is 720kVA compared with 900kVA for the NPC. The components of the NPC will stay cooler so that a comparison at Tjmax will show that the components could be used at higher currents. With a optimization of the chip size to the same Tjmax at the same power, the NPC module will be significantly lower in cost than a standard half bridge component. The dditional advantages in reduced EMC and increased efficiency are on top.
The mixed voltage 3 level topology achieves the same efficiency as the standard NPC but it have to provide a higher effort for the semiconductor of 1080kVA compared with 900kVA of the NPC.